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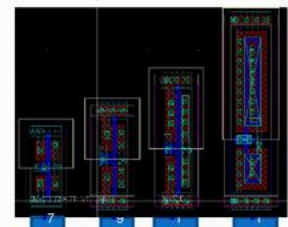
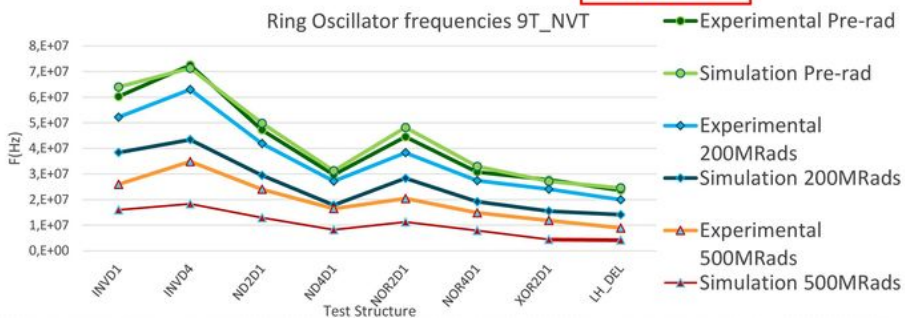
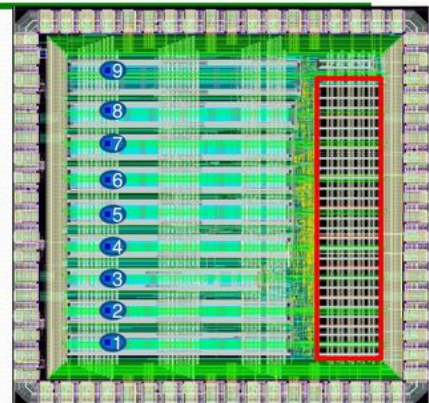
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## DRAD Chip : Test chip for digital design

- ❑ DRAD chip is designed at CERN :
- ❑ To study the effect of radiation on digital standard cells for the 65nm TSMC technology
- ❑ To test the efficiency and the validity of the digital simulations with the irradiation corner model
- ❑ Simulation results goes in the same direction than irradiation tests but the model overestimates the TID damage level
  - Models were done for worst case of biasing
- ❑ NOR gates should be avoided since show a strong degradation

**ANNEALING  
NOT  
INCLUDED  
IN THE  
MODELS**



**CELL HEIGHT**  
7 Track: 1.4  $\mu\text{m}$   
9 Track: 1.8  $\mu\text{m}$   
12 Track: 2.4  $\mu\text{m}$   
18 Track: 3.6  $\mu\text{m}$

April 6, 2017

AIDA2020 - 2nd Annual Meeting -

7

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